Future Computing with the Rogues Gallery

1st Aaron Jezghani
Partnership for an Adv. Comp. Env.
Georgia Institute of Technology
Atlanta, United States
0000-0002-4302-4227

2nd Jeffrey Young
School of Computer Science
Georgia Institute of Technology
Atlanta, United States
0000-0001-9841-4057

3rd Will Powell
School of Comp. Science and Eng.
Georgia Institute of Technology
Atlanta, United States
0000-0002-1570-5930

4th Ronald Rahaman
Partnership for an Adv. Comp. Env.
Georgia Institute of Technology
Atlanta, United States
0000-0002-8917-8934

5th J. Eric Coulter
Partnership for an Adv. Comp. Env.
Georgia Institute of Technology
Atlanta, United States
0000-0001-6710-9244

***Abstract*—The Vertically Integrated Projects (VIP) Program at Georgia Tech provides a multidisciplinary research experience aimed at engaging undergraduate and graduate research students in large-scale computing research projects. Since 2019, the Future Computing with the Rogues Gallery VIP course has engaged over 75 students in research on topics related to novel architectures and "post-Moore" computing platforms built around quantum, neuromorphic, near-memory, and reconfigurable computing.**

One of the key takeaways from this course for the course designers has been on the correlation between these novel computing platforms and traditional skills, techniques, and tools that are used in the HPC and parallel computing arenas. We discuss these parallels as well as the impacts of this course on general student success and research outcomes.

***Index Terms*—undergraduate education, parallel computing, novel architecture testbeds, student-oriented research**

I. Introduction

Key areas of focus for teaching parallel computing are typically targeted towards teaching the algorithms, data structures, and hardware accelerators that can be used to execute applications in a parallel or distributed environment. At the same time, we are increasingly seeing more cheap, novel architectures like Xilinx's Pynq Z2 Field Programmable Gate Arrays (FPGAs) that can be used by students for coursework to implement parallel versions of algorithms and highly parallel deep neural networks. Taking these novel architectures to the extreme, we also foresee more future-looking parallel systems that have not yet been explored in the classroom outside of limited graduate special topics courses. These "post-Moore" technologies are ones that engage in a large paradigm change to the traditional computing structure whether it is through computing with qubits, as with quantum computing or using brain-inspired spiking neural networks, as with neuromorphic computing.

The NSF-funded CRNCH Rogues Gallery (RG) testbed [1], [2] at Georgia Tech provides a unique environment that specifically targets "post-Moore" computing as well as next-generation parallel architectures based on CPUs, GPUs, and FPGAs. With access provided to students, faculty, and industry collaborators, the Rogues Gallery provides users the opportunity to explore and understand these new architectures within a managed datacenter environment with common identity management, networking, and storage.

From an educational perspective, the Rogues Gallery also serves as a touchpoint for novel architecture research and exploration that is not currently served by Georgia Tech's other HPC infrastructure, like PACE's ICE and Phoenix clusters (see section II-C). As new architectures move from "novel" to mainstream, we anticipate that educational and research applications will also change to serve a larger audience of students and researchers. Two demonstrative examples are the last ten years of growth of GPUs as an HPC and parallel computing platform and the more recent introduction of new parallel processors from Arm and RISC-V vendors [3].

As the deployment of this unique testbed resource has progressed, we have also focused on supporting student research via a Vertically Integrated Projects [4] class called Future Computing with the Rogues Gallery, or the Rogues Gallery VIP for short. This class has been beneficial for students but has also provided a few surprises for the instructors of this course and the maintainers of the RG testbed. We explain these aspects in more in depth in the following sections but note the following high-level takeaways:

- As might be expected, traditional parallel computing and HPC frameworks and tools tend to provide a good entry point for students to engage with unique architectures by lowering the bar to engagement. We supplement this with the concept of novel architecture workflows that mirror traditional HPC workflows (section II-A).
- Integration of the "novel" and "traditional" aspects of parallel computing for new architectures also eases the burden of deploying new architectures, although it requires planning and coordination to do so properly (section II-C).
- Students in the VIP class typically enter with a low amount of domain-specific knowledge but student feedback and enrollment shows that engagement and learning

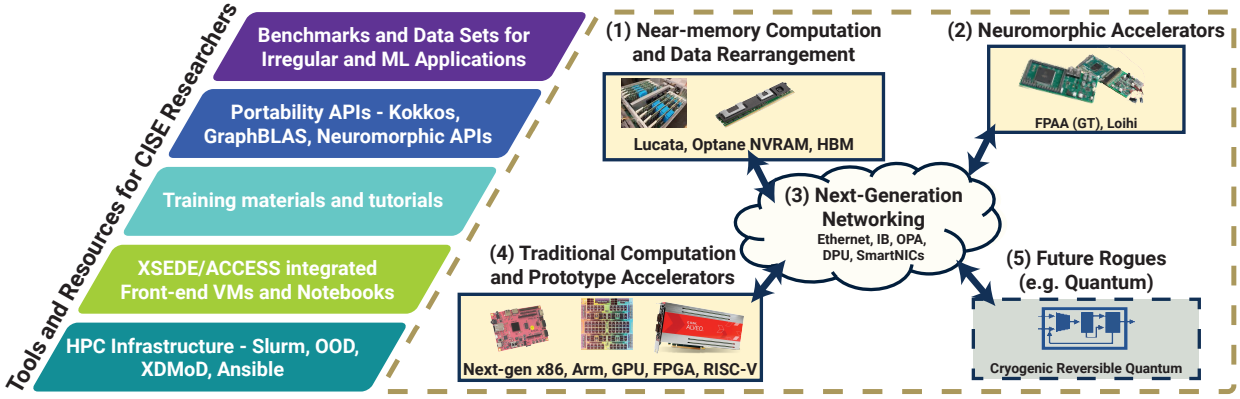

Fig. 1. Overview of the Rogues Gallery Testbed Along with Related Tools, Frameworks, Infrastructure, and Training Resources.

outcomes increases dramatically over their tenure with the class (section IV).
- The deployment of a unique VIP class for novel architectures also helps to address a "missing middle" in terms of teaching students about parallel and novel computing constructs before they might normally be encountered in a standard course of study (section III-E).

II. The Rogues Gallery: A Post-Moore Computation Testbed

The Rogues Gallery testbed was founded in 2017, and it has gradually grown from one near-memory server [5] to an NSF CISE Community Research Infrastructure funded effort that contains 15+ servers, multiple standalone dev boards, a 64-node FPGA cluster, and approximately 10 virtual machines for development. In addition to NSF funding, hardware for the Rogues Gallery was procured through Sandia sponsorship and Georgia Tech's Tech-Fee Fund initiative.

Figure 1 shows a high-level overview of the current testbed, as deployed via the CCRI program. Five general areas of novel architectures are supported including: 1) near-memory accelerators - devices that perform computation close to or in memory and storage, 2) neuromorphic accelerators - brain-inspired and spiking neural network hardware like Georgia Tech's FPAA [6], 3) smart networking devices like NVIDIA's BlueField along with high-speed networks, 4) "traditional" HPC-style accelerators like FPGAs, GPUs, and Arm/RISC-V processors, and 5) simulators and emulators for future devices using cryogenic CMOS, or reversible or quantum computing. While quantum computing research efforts provide a foundation for our fifth thrust area, no quantum hardware is currently incorporated in the RG.

Architectures available in the testbed include:

- Lucata Pathfinder migratory-thread compute systems
- Intel Optane DCPMM and SSDs
- Intel and Xilinx field programmable gate arrays (FPGAs)
- Xilinx Zynq system-on-chip (SoC) boards
- Field-programmable analog arrays (FPAAs) for neuromorphic processing
- FPGA- and DPU-based SmartNICs
- Next-gen x86, Arm, and GPU processors
- Ethernet, OmniPath, and InfiniBand interconnects

Notable to our concept of a testbed is the focus on the tools, tutorials, and frameworks that are used to access and program these novel architectures. As an example, the GraphBLAS API is supported on the Lucata Pathfinder while Kokkos provides a parallel portability API for CPUs and GPUs that can possibly be extended for other parallel architectures like FPGAs.

A. Iterative Workflow on the RG

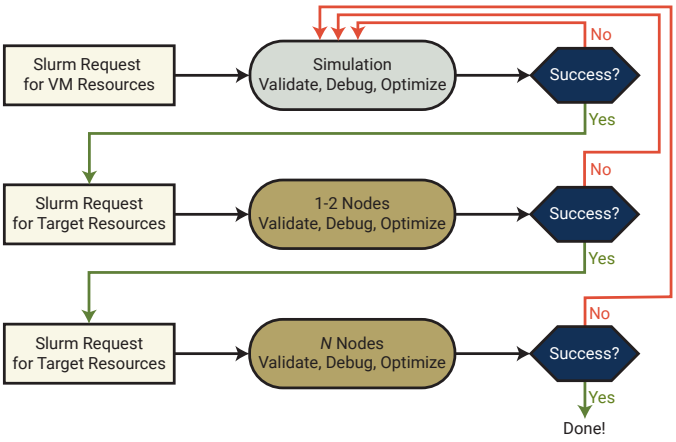

Fig. 2. Generalized workflow for RG systems. After testing code on x86 development VMs, users proceed to scaling on the target architecture, repeating x86 debugging as appropriate.

As an educational resource, many of the novel architectures in the Rogues Gallery can be challenging to undergraduate students who may not have encountered parallel computing or resources like Linux-based clusters. One of the key focuses of the Rogues Gallery VIP class is on breaking down complex workflows for novel architectures into simpler steps.

Figure 2 shows a generalized workflow that closely mirrors the standard parallel computing workflow students might engage with. As an example, a student might be tasked to develop a new breadth-first search algorithm using the "near-memory" Lucata Pathfinder system and its Cilk programming

environment from fig. 1. As a first step, these students would request a standard x86 virtual machine environment for emulation, where the algorithm runs on the x86 CPU, or a simulation environment, where the algorithm runs on a simulated model of the target hardware. As part of this step, students would engage in standard debugging and profiling as provided by the Lucata programming and tools environment. Once the functional performance is correct, the student uses Slurm to request 1-2 nodes on the Pathfinder system to test scalability and then N nodes to do performance analysis. In an ideal case, this workflow would be supplemented by appropriate tutorial notebooks and example codes that students could use as templates for their own projects and research.

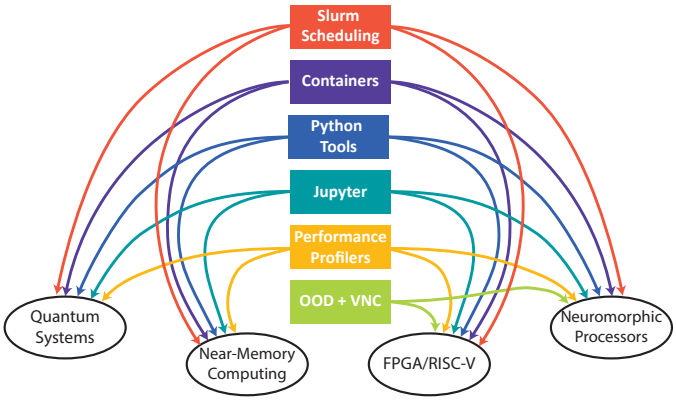

Fig. 3. Mapping traditional HPC applications and infrastructure to novel hardware.

B. Administration through Enterprise Solutions

This focus on an HPC-style workflow for novel architecture environments extends from this initial workflow to a more complex set of HPC infrastructure resources that can be used to fully support diverse student projects and research topics. Figure 3 shows the four main areas of research for our Rogues Gallery VIP class along with the traditional HPC infrastructure that supports each area of research. These topic areas are described in more detail in section III but they broadly cover quantum, near-memory, and neuromorphic computing as well as reconfigurable and RISC-V architectures. Most of the novel architectures for these research areas have some sort of a Python front-end or interface, so we support Python tools as well as Jupyter notebooks for application devleopment and student tutorials and training [7]. At the same time, some research areas like reconfigurable computing also make usage of GUI-based tools like Xilinx's Vivado and Vitis. As described in a related publication on our FPGA cluster implementation [8] in 2022, these students interact with the cluster environment via a combination of Open OnDemand and related VNC plugins.

C. Collaboration with PACE

As a final component of the Rogues Gallery testbed's support for student coursework, we note that HPC integration for this novel architecture testbed is dependent on a close collaboration with our local HPC group, the Partnership for Advanced Computing Environments (PACE). PACE maintains local Instructional Computing Environments (ICE) collaboratively with the College of Computing (CoC-ICE) and for general campus users (PACE-ICE) [9]. CoC-ICE is a dedicated instructional HPC cluster administered as a collaboration between the College of Computing (CoC) and PACE that is used to host courses in computing and electrical engineering. PACE-ICE supports courses that teach and use scientific computing in engineering, physical and social sciences, and humanities and arts, and it is also used for training workshops offered by PACE to the entire campus community.

The existence of these ICE environments is a key piece of why the Rogues Gallery can be successful as an educational tool. As described in greater detail in [8], the CRNCH Rogues Gallery testbed can be used in conjunction with CoC-ICE to allow students to run the first part of a novel architecture workflow on a traditional HPC cluster. Specifically, students can use a large HPC node on CoC-ICE to launch multiple instances of the "simulation" phase for a reconfigurable computing flow in a processor design course, and they can then migrate their project to the RG testbed to evaluate their designs on remotely accessible FPGA hardware.

As an added bonus to this synergistic pipeline for student projects, both CoC-ICE and the RG testbed make use of the same tooling and environment. Both systems share similar modular software stack, Slurm deployment strategies, and Open OnDemand configurations, which makes maintenance of the testbed and prototyping of new features more seamless and sustainable. Furthermore, containerized software solutions leverage the same Apptainer (formerly Singularity [10]) workflow to directly port scaled efforts to CoC-ICE, or even Phoenix, PACE's flagship research cluster.

III. Future Computing with the Rogues Gallery VIP

The Vertically Integrated Projects [4], or VIP program has been active since the late 1990s as a model for undergraduate research with a focus on engaging more students in research projects. VIP teams are meant to be 1) multidisciplinary with participants from across departments on campus, 2) vertically integrated with both newer and more senior students, 3) large-scale with 10 or more participants per team, and 4) long-term with students participating for three or more semesters. Specifically, VIP is targeted at reducing barriers to meaningful research experiences. Georgia Tech is host to over 80 VIP teams, and over 40 institutions world-wide are part of a consortium of VIP sites.

Students typically engage with a VIP team for three semesters. In some colleges, (e.g., the College of Computing) VIP is offered as an alternative to Georgia Tech's traditional junior design course, which makes it an attractive option for many undergraduate students. At the same time, masters students are also welcome to use VIP courses to satisfy some of their elective credits. Some of the VIP classes with similar profiles to the Rogues Gallery VIP class include other

courses focused on reconfigurable computing ("Configurable Computing & Embedded Systems" [11]), autonomous vehicles ("Active Safety for Autonomous and SemiAutonomous Vehicles" [12]), and novel networking ("Agile Communication Architectures" [13]).

Future Computing with the Rogues Gallery The Rogues Gallery VIP, was started in the Fall semester of 2019. The initial vision for this course was to provide students a venue to work with prototype FPGAs, near-memory accelerators, and HPC hardware. Two instructors from the College of Computing, Dr. Jason Riedy and Dr. Jeffrey Young, taught a class of nine students for this initial semester. One early surprise for the course was the strong student interest in quantum computing hardware and programming, which led to a subteam being formed solely around quantum computing topics.

We briefly review some of the projects each subteam has focused on and note that student projects are featured in more detail on our class website [14].

A. Near-Memory Subteam

The earliest subteam for the Rogues Gallery VIP class is based around the concept of near-memory computing with the Lucata Pathfinder system [15]. On this platform, students use the parallel Cilk language [16] to program algorithms related to graph and sparse data analytics. A key requirement for these students is a basic understanding of parallel computing clusters, as the Pathfinder system is a multi-core, multi-node, and multi-chassis platform. We have found that resources like LLNL's Introduction to Parallel Computing tutorial [17] and Cilk tutorials are key starting points for students to engage with this subteam.

B. Neuromorphic Subteam

The neuromorphic subteam is focused on multiple projects related to Simultaneous Location and Mapping (SLAM), a technique for autonomous vehicles and robots. One long-running project, "NeuroCar" looks to build a spiking neural network version of an autonomous racecar, and it has recently engaged recent research in the field like insights from the RatSLAM project [18]. Newer projects have also started to look at using energy-efficient spiking neural networks (SNNs) and hardware like Intel's Loihi [19] for tasks related to image processing. All of these projects tend to be parallel in nature in that they mirror standard neural network workflows, and students often need to learn or brush up on their knowledge of key topics like backpropagation to fully engage with the subteam's projects.

One key item to note is that this subteam independently has developed some of its own training materials and starter projects. As an example, new students typically learn about the Nengo [20] neuromorphic framework and use it to implement a maze navigation sub-problem with a very simple SNN. Related student starter projects have focused on solving problems from the OpenAI Gym environment [21].

C. Reconfigurable Subteam

The reconfigurable subteam is generally focused on reconfigurable, FPGA-based architectures to implement new and interesting accelerators. Two key decisions were made in forming this subteam: 1) Students typically will work using a high-level language like Chisel [22] or a framework like Vitis HLS rather than writing Verilog code directly. 2) Most research projects focus on some aspect of RISC-V design through the publicly available Chipyard [23] and PULP [24] projects. Students have looked at developing AES encryption and ML-focused accelerators that can be run and modified on standard Xilinx FPGAs.

These suggested ground rules for the initial reconfigurable subteam formulation were made in part because other course curriculum at Georgia Tech covers standard Verilog design and because we felt that working with a widely available framework like PULP or Chipyard would allow students to explore how their accelerators worked within a larger ecosystem.

D. Quantum Computing Subteam

While quantum computing hardware is still relatively rare and limited in availability, the basics of quantum computing are easily accessible through many online tutorials and textbooks including the classic Nielsen and Chuang book [25] and the widely referenced Qiskit documentation and interactive textbook [26], [27]. At the same time, the details of quantum algorithm development, quantum mechanics, and quantum theory are extremely complex due to the incorporation of concepts from computing, materials and devices, linear algebra, and physics. Many students in this subteam spend the first semester just getting up to speed on the basic concepts of quantum computing while returning students investigate topics related to the application of ML to reduce noise in quantum circuits and on parallel computing techniques to accelerate quantum simulation with tools like NVIDIA's cuQuantum or the parallel TNQVM simulation framework [28].

E. Comparison with Other Parallel Computing Training

For all the subteams in the Rogues Gallery VIP we note that there are clear consistencies with other parallel computing training and courses. As we noted in section II-A, many of the novel architectures in the Rogues Gallery testbed follow a similar workflow where simulation or emulation is followed by single-node and multi-node execution on actual hardware. Secondly, many of the topics covered in this course depend on the usage of parallel computing frameworks, whether that is TensorFlow for machine learning training with neuromorphic and quantum projects, Cilk for the Lucata Pathfinder, or parallel kernel deployment using reconfigurable tools like Xilinx's Vitis HLS. By drawing comparisons and contrasts between each area, we help students to build skill sets that are translatable from one novel architecture to another (e.g., using knowledge about neural networks to address parallel computation on similar graph data structures with the Pathfinder system and vice versa).

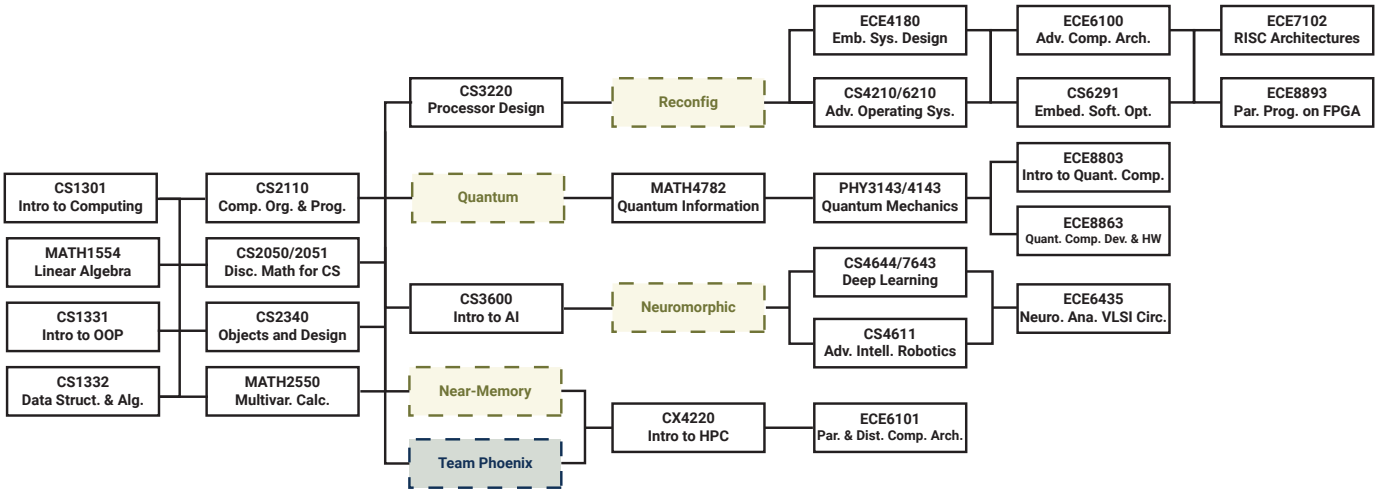

Fig. 4. The Rogues Gallery VIP addresses the "Missing Middle" of Novel Architectures and Parallel Computing, with the different subteams highlighted in yellow in each topical curriculum. Additionally, the Team Phoenix VIP highlighted in blue provides a deeper dive into traditional HPC topics.

Importantly, we have found that this VIP course helps to fill a "missing" segment of instruction for other courses in the Georgia Tech computing curriculum. All of the students in our course benefit from a good background in linear algebra, which is critical to have a clear understanding of the workings of neural networks, near-memory and cluster computing, and quantum computing topics. Several of the subteams also provide an early introduction to topics like quantum information science or high-performance computing applications that would normally be covered in senior-level courses. This is notable in that as section IV shows, a large number of students engage with VIP courses when early in their collegiate career. A related VIP course for our student cluster competitition team, "Team Phoenix" [29], shares overlap with the near-memory subteam in its focus on parallel computing concepts, and it also provides an early entry point for students to engage with distributed and parallel systems early in their undergraduate career.

F. Collaborative Development of Training Materials

A useful collaborative effort for the Rogues Gallery VIP class is the engagement of students in related training efforts for the Rogues Gallery testbed that then leads to new "getting started" materials for new students to the course.

The Lucata tutorial at HPEC 2022 [7] was the first tutorial that made use of newly deployed capabilities for Open OnDemand on the RG testbed as well as detailed Jupyter notebooks that could be used to implement the simulation, single-node, and multi-node workflows described in section II-A. The development of this tutorial provided both a learning opportunity for near-memory VIP students as well as a valuable source of feedback on how to best improve training materials for this complex architecture to make it more approachable to students.

Similarly, the Vortex tutorial at MICRO 2022 [30] was not officially part of the VIP course, but the development and deployment of this tutorial created new software tools, HPC scheduler integrations, and documentation on how students could run both verilator based examples on their laptop as well as how they could migrate these initial examples to the Rogues Gallery testbed for longer simulations.

IV. Course Efficacy

As part of the VIP program, grades are calculated as 33% Documentation, 33% Teamwork, and 33% Accomplishments & Contributions [31]. For the Rogues Gallery VIP, each student is required to maintain a markdown file in Github with weekly updates to satisfy the first criterion; midterm grades are provided with feedback to guide students to detailed and meaningful notebook entries as the semester progresses. Additionally, students complete peer evaluations at the middle and end of semester, through which they rank their subteam peers in terms of technical contributions and leadership capabilities. The results of these surveys are then forwarded to the instructors who utilize them to assess an individual's participation within their respective subteam. Lastly, the semester culminates with a research poster presented by each subteam to evaluate their technical achievements over the course of the semester.

A. Growth in Enrollment

Figure 5 shows the total number of students by semester and the breakdown by academic rank. The VIP course has seen increasing enrollment, with total students reaching an instructor-imposed limit of 35 students. This limit is largely meant to effectively manage the class and provide appropriate faculty mentorship across the subteams. In all semesters, students span all ranks, and often continue with the course for multiple semesters. In this way, the "vertical" component of the the VIP program is demonstrably realized within the Rogues Gallery VIP course, as these experienced students readily adopt the roles of subteam leaders.

As of this semester, this VIP course has had 83 unique student participants from seven different majors (computer

science, computer engineering, electrical engineering, mathematics, physics, literature, media, and communication (LMC), and industrial systems and engineering (ISyE).

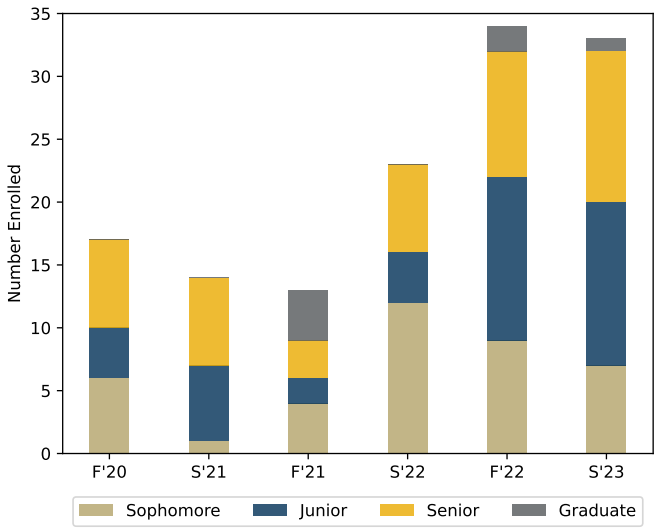

Fig. 5. Course enrollment by semester.

B. Student Feedback

In 2020, all VIP courses had the Course-Instructor Opinion Survey (CIOS) added to the end of their normal course structure. The anonymous survey is comprised of three sections: Student Effort, Quality of Course, and Quality of Teaching, each with a mix of frequency scale (FS), Likert scale (LS), and free response (FR) questions. The keys for the numeric ranking of values changes with each question, but in general the values range from 1 to 5, with 1 corresponding to the least positive response and 5 indicating the most positive response. To assess the efficacy of the Rogues Gallery VIP course, a subset of the CIOS questions can be considered:

1) Student Effort
   a) (FR): Comments about your effort (eg., - was the expected and expended effort appropriate for this course?).
2) Quality of Course
   a) (LS): Rate how prepared you were to take this subject.
   b) (LS): How much would you say you learned in this course?
   c) (LS): Considering everything, this was an effective course.
   d) (FR): What were the best features of the course, such as lectures, activities, assignments, and projects?
   e) (FR): How could this course be improved?

Figure 6 summarizes the results of questions 2a, 2b, and 2c since the CIOS was introduced. Despite a self-reported sense of less-preparedness for the course, students resoundingly provided positive feedback in terms of the amount learned and overall course efficacy. Comparing these results to the open-ended responses to questions 1a and 2e, the sophomores often reported more time invested and initial hurdles adapting to a research-focused course. In comparison, responses provided by higher rank students aligned effort more closely to enrolled credits. Suggestions from all ranks generally indicated a need for more extensive documentation and training material.

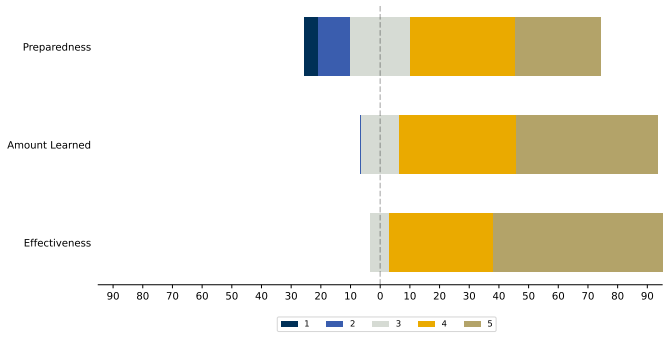

Fig. 6. Aggregate CIOS responses for questions 2a, 2b, and 2d since Fall 2020. The Likert scale runs from 1 to 5, where 5 aligns with the most positive sentiment and 1 the least.

Exploring student feedback further, Figure 7 visualizes the results of question 2d as a word cloud. As the VIP course often provides many students their first exposure to research-based tasks, students overwhelmingly agreed that their independence and the project-based workflow were the best features of the course. Other noteworthy feedback from students included an appreciation for the self-driven learning through hands-on activity as well as the pride after finalizing a professional publication and subsequent presentation.

Fig. 7. Word map highlighting common terms in student responses to question 2d. Broadly speaking, a general appreciation for self-paced study through the task-based research teams was expressed by many students.

V. Course Replication at Other Institutions

To reproduce a course such as the Rogues Gallery VIP, two separate components should be addressed: (1) the VIP course infrastructure and (2) the compute hardware. Fortunately, the first and most critical component is readily addressed through the VIP Consortium's information for new sites [32], which details pathways to start a VIP program, ideal course structure, faculty and student recruitment, and academic policies. Although graduate students play a critical role in mentoring incoming students, as they typically bring an experienced background from prior years on the team, advanced coursework, or industry experience, the VIP infrastructure is still applicable at undergraduate institutions, as multiple semesters of participation provide a good foundation for onboarding new team members. These experienced students mitigate a portion of the effort for the course instructor, which is critical given the inherent challenges in introducing an array of novel compute architectures at an early stage in students' academic careers.

As for hardware procurement, instructors can reasonably choose a single platform as a starting point from which a broader array of architectures can be explored. The Rogues Gallery VIP was initially developed around the Lucata near-memory hardware, although several subteams now leverage more affordable solutions based on the Pynq boards or even software- and cloud-based quantum resources. Aside from cost-efficiency, this approach also aids in time-management, as instructors can build student expertise for a semester or two to afford themselves an opportunity to explore additional architectures and expand subteam offerings.

VI. Summary

The prognosis for the Future Computing with the Rogues Gallery VIP seems to be promising based on the first three years of the course and related tool and training development that has enhanced the Rogues Gallery testbed and its community. Our ideal goal for this course would be to continue to grow the basic training for students so that they could show up with a limited amount of base knowledge and then work through a set of "getting started" notebooks to get up to speed. In fact, current plans for a related Online Master of Science in Computer Science (OMSCS) course [33] on post-Moore computing may provide a basis for completing these initial resources for undergraduates and graduates alike. At the same time, we look to further explore and extend the connections between traditional parallel computing techniques and architectures and these new and novel platforms.

VII. Acknowledgment

This work was supported by the NSF MRI award #1828187: "MRI: Acquisition of an HPC System for Data-Driven Discovery in Computational Astrophysics, Biology, Chemistry, and Materials Science." Additionally, this work was supported in part through research infrastructure and services provided by the Rogues Gallery testbed hosted by the Center for Research into Novel Computing Hierarchies (CRNCH) at Georgia Tech. The Rogues Gallery testbed is primarily supported by the National Science Foundation (NSF) under NSF CCRI Award Number #2016701. Any opinions, findings and conclusions, or recommendations expressed in this material are those of the author(s), and do not necessarily reflect those of the NSF.

References

[1] J. S. Young, J. Riedy, T. M. Conte, V. Sarkar, P. Chatarasi, and S. Srikanth, "Experimental insights from the rogues gallery," in *2019 IEEE International Conference on Rebooting Computing (ICRC)*, Nov 2019, pp. 1–8.

[2] W. Powell, J. Riedy, J. S. Young, and T. M. Conte, "Wrangling rogues: A case study on managing experimental post-moore architectures," in *Proceedings of the Practice and Experience in Advanced Research Computing on Rise of the Machines (Learning)*, ser. PEARC '19. New York, NY, USA: ACM, 2019, p. 61:1–61:8. [Online]. Available: http://doi.acm.org/10.1145/3332186.3332223

[3] A. Jezghani, K. Manalo, W. Powell, J. Valdez, and J. Young, "Onboarding users to a64fx via open ondemand," in *International Conference on High Performance Computing in Asia-Pacific Region Workshops*, 2022, pp. 78–83.

[4] S. Marshall, E. Coyle, J. V. Krogmeier, R. T. Abler, A. Johnson, and B. E. Gilchrist, "The vertically integrated projects (vip) program: leveraging faculty research interests to transform undergraduate stem education," in *Transforming Institutions: 21st Century Undergraduate STEM Education Conference*, 2014.

[5] E. R. Hein *et al.*, "Programming strategies for irregular algorithms on the emu chick," *ACM Transactions on Parallel Computing (TOPC)*, vol. 7, no. 4, pp. 1–25, 2020.

[6] S. George *et al.*, "A programmable and configurable mixed-mode fpaa soc," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 6, pp. 2253–2261, 2016.

[7] CRNCH, "CRNCH HPEC 2022 Lucata Pathfinder tutorial page," 2022. [Online]. Available: https://github.com/gt-crnch-rg/lucata-pathfinder-tutorial/

[8] J. Young *et al.*, "Enhancing hpc education and workflows with novel computing architectures," *Journal of Computational Science*, vol. 13, no. 2, 2022.

[9] M. Belgin *et al.*, "Ice: A federated instructional cluster environment for georgia tech," in *Proceedings of the Practice and Experience on Advanced Research Computing*, ser. PEARC '18. New York, NY, USA: Association for Computing Machinery, 2018. [Online]. Available: https://doi.org/10.1145/3219104.3219112

[10] G. M. Kurtzer, cclerget, M. Bauer, I. Kaneshiro, D. Trudgian, and D. Godlove, "hpcng/singularity: Singularity 3.7.3," Apr. 2021. [Online]. Available: https://doi.org/10.5281/zenodo.4667718

[11] L. Lerner, M. Ruiz, and W. Stucky, "Configurable Computing & Embedded Systems VIP Webpage," 2023. [Online]. Available: https://www.vip.gatech.edu/teams/vpz

[12] P. Tsiotras and K. Feigh, "Active Safety for Autonomous and SemiAutonomous Vehicles VIP Webpage," 2023. [Online]. Available: https://www.vip.gatech.edu/teams/vvb

[13] M. Bloch, "Agile Communication Architectures," 2023. [Online]. Available: https://www.vip.gatech.edu/teams/vw3

[14] J. Young and A. Jezghani, "Future Computing with the Rogues Gallery," 2023. [Online]. Available: https://gt-crnch-rg.github.io/fc-with-rg-vip/

[15] T. Dysart *et al.*, "Highly scalable near memory processing with migrating threads on the emu system architecture," in *2016 6th Workshop on Irregular Applications: Architecture and Algorithms (IA3)*, 2016, pp. 2–9.

[16] T. B. Schardl, I.-T. A. Lee, and C. E. Leiserson, "Brief announcement: Open cilk," in *Proceedings of the 30th on Symposium on Parallelism in Algorithms and Architectures*, ser. SPAA '18. New York, NY, USA: Association for Computing Machinery, 2018, p. 351–353. [Online]. Available: https://doi.org/10.1145/3210377.3210658

[17] B. Barney and D. Frederick, "Introduction to Parallel Computing Tutorial," 2023. [Online]. Available: https://hpc.llnl.gov/documentation/tutorials/introduction-parallel-computing-tutorial

[18] M. Milford, G. Wyeth, and D. Prasser, "Ratslam: a hippocampal model for simultaneous localization and mapping," in *IEEE International Conference on Robotics and Automation, 2004. Proceedings. ICRA '04. 2004*, vol. 1, 2004, pp. 403–408 Vol.1.

[19] C.-K. Lin *et al.*, "Programming spiking neural networks on intel's loihi," *Computer*, vol. 51, no. 3, pp. 52–61, 2018.
[20] T. Bekolay *et al.*, "Nengo: a python tool for building large-scale functional brain models," *Frontiers in Neuroinformatics*, vol. 7, 2014. [Online]. Available: https://www.frontiersin.org/articles/10.3389/fninf.2013.00048
[21] G. Brockman *et al.*, "Openai gym," *arXiv preprint arXiv:1606.01540*, 2016.
[22] J. Bachrach *et al.*, "Chisel: constructing hardware in a scala embedded language," in *Proceedings of the 49th Annual Design Automation Conference*, 2012, pp. 1216–1225.
[23] A. Amid *et al.*, "Chipyard: Integrated design, simulation, and implementation framework for custom socs," *IEEE Micro*, vol. 40, no. 4, pp. 10–21, 2020.
[24] P. D. Schiavone, D. Rossi, A. Pullini, A. Di Mauro, F. Conti, and L. Benini, "Quentin: an ultra-low-power pulpissimo soc in 22nm fdx," in *2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, 2018, pp. 1–3.
[25] M. A. Nielsen and I. Chuang, "Quantum computation and quantum information," 2002.
[26] A. tA v *et al.*, "Qiskit: An open-source framework for quantum computing," 2021.
[27] J. R. Wootton, F. Harkins, N. T. Bronn, A. C. Vazquez, A. Phan, and A. T. Asfaw, "Teaching quantum computing with an interactive textbook," in *2021 IEEE International Conference on Quantum Computing and Engineering (QCE)*, 2021, pp. 385–391.
[28] A. McCaskey, E. Dumitrescu, M. Chen, D. Lyakh, and T. Humble, "Validating quantum-classical programming models with tensor network simulations," *PloS one*, vol. 13, no. 12, p. e0206704, 2018.
[29] S. Bryngleson, W. Powell, J. Valdez, and R. Vuduc, "Team Phoenix VIP Webpage," 2023. [Online]. Available: https://gt-chipc.github.io/gt-student-cluster-competition/
[30] B. Tine, H. Kim, and J. Young, "Vortex 2022 tutorial page," 2022. [Online]. Available: https://github.com/gt-crnch-rg/vortex_tutorials
[31] "Graded Categories - VIP Site Resources," https://sites.gatech.edu/vipsiteresources/graded-categories/, Accessed: 2023-03-15.
[32] "VIP Site Resources," https://sites.gatech.edu/vipsiteresources/, Accessed: 2023-03-15.
[33] Z. Galil, "OMSCS: The revolution will be digitized," *Communications of the ACM*, vol. 63, no. 8, pp. 27–29, 2020.